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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 23/498 A1

(11) International Publication Number: WO 99/17364

(43) International Publication Date: 8 April 1999 (08.04.99)

(21) International Application Number: PCT/US98/20467

(22) International Filing Date: 29 September 1998 (29.09.98)

(30) Priority Data:
939,832 29 September 1997 (29.09.97) US

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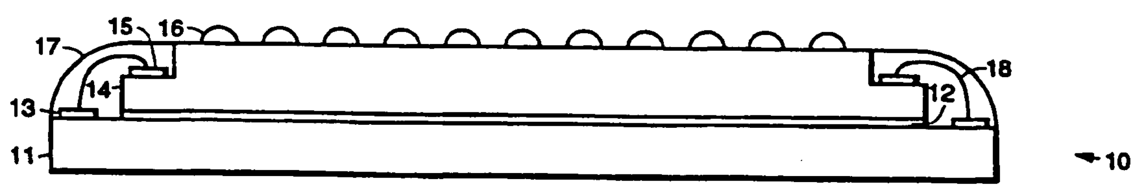
(81) Designated States: CA, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: CHIP-SIZE PACKAGE USING A POLYIMIDE PCB INTERPOSER



(57) Abstract

A chip-size package formed using a printed circuit board, preferably comprising polyimide. The chip-size package comprises an integrated circuit chip having a plurality of peripheral bond pads. The printed circuit board has a plurality of solder bumps formed on its top surface and a plurality of bond pads around its periphery. A layer of adhesive is used to secure the printed circuit board and the integrated circuit chip together. A plurality of wire bonds electrically connected between selected bond pads of the integrated circuit chip and the printed circuit board. An encapsulant encapsulates the wire bonds and bond pads of the integrated circuit chip and the printed circuit board.

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CHIP-SIZE PACKAGE USING A POLYIMIDE PCB INTERPOSER

BACKGROUND

The present invention relates generally to integrated circuit packages and methods. and more particularly, to a chip-size integrated circuit package formed using a polyimide printed circuit board interposer.

The closest form of art to the present invention is a chip-size package made by a company called Tessera. The Tessera chip-size package uses formed tape automated bonded (TAB) lead frames on a polyimide film. It would be desirable to have a chip-size package that has fewer processing steps, is less expensive to build. and that employs commonly available processing equipment.

Furthermore, most chip size package designs are larger than the die itself. It would therefore be desirable to have a chip-size package that packages the integrated circuit chip within the internal surface area of the bare die.

Accordingly, it is an objective of the present invention to provide for an improved chip-size package formed using a polyimide printed circuit board interposer.

SUMMARY OF THE INVENTION

To meet the above and other objectives. the present invention provides for a chip-size package formed using a polyimide printed circuit board interposer. It is believed that the present invention may be built for a lower cost than the Tessera or other prior art chip-size package because the present invention has fewer processing steps and has a lower material cost. The present invention also uses more common and lower cost processing equipment than does the Tessera or other prior art process.

The present invention converts a single, unpackaged bare silicon chip into a packaged chip no larger in area than the bare chip. The present invention uses readily available printed circuit board materials and technology. This chip size packaging scheme of the present invention is novel in that it uses a low cost printed circuit board interposer with exposed, lower layers incorporating wire bond pads. The wire bond pads are sufficiently lower than the solder bumps on the top layer of the interposer, and as such, wire bonds to the wire bond pads can be encapsulated without exceeding the height of the top printed circuit board layer which must remain flat for soldering.

The present invention converts a bare chip into a chip size package. The chip size package may be assembled in a manner similar to surface mount devices which are soldered to printed circuit boards. Chip size packages, however, take up only 10-20% of the area of conventionally packaged chips fabricated as surface mount devices. Development of the chip size package of the present invention is an important step in achieving miniaturization of microelectronics.

Most chip size packages are larger than the die itself. The present invention however, packages the chip within the internal surface area of the bare die. Because the present chip size package takes up no additional area than the bare die, it is believed to be the smallest two-dimensional integrated circuit package that has yet been developed.

The benefit of converting a bare die into a surface mount device is that it provides mechanical and environmental protection for the fragile silicon integrated circuit chip. The present invention also converts a fine pitch peripheral pad integrated circuit into a packaged, courser pitch area array device, permitting it to be easily tested, burned in, and assembled to standard printed circuit boards using existing, common equipment used in the industry. The ability to use "known good" tested devices while utilizing industry standard and accepted equipment and processes is a key element in obtaining the absolute lowest product cost.

The present invention permits silicon integrated circuits to be packaged in the smallest area possible, which is no larger than the size of the integrated circuit itself. Incorporating such low cost integrated circuit packages into various microelectronic applications will provide for smaller product sizes, lower weight, and lower assembly and testing costs. The present invention provides for a robust packaging structure that is suitable for a variety of commercial and military applications, including automotive electronics, for example.

BRIEF DESCRIPTION OF THE DRAWINGS

The various features and advantages of the present invention may be more readily understood with reference to the following detailed description taken in

conjunction with the accompanying drawings. wherein like reference numerals represent like structural elements. and in which:

Fig. 1a-1c illustrate formation of a chip-size integrated circuit package in accordance with the principles of the present invention:

Fig. 2 is a perspective view of a fully assembled chip-size integrated circuit package; and

Fig. 3 illustrates the chip-size integrated circuit package assembled to a printed circuit board.

DETAILED DESCRIPTION

Referring to the drawing figures. Fig. 1a-1c illustrate formation of a chip-size integrated circuit package 10 in accordance with the principles of the present invention. Referring to Fig. 1a. the chip-size integrated circuit package 10 comprises an integrated circuit chip 11. which may be a silicon integrated circuit chip 11. for example. having a plurality of peripheral bond pads 13. A printed circuit board 14. or interposer 14. which is preferably comprised of polyimide. is formed having a plurality of solder bumps 16 (or an area array of solder bumps 16) formed on a top surface. and a plurality of bond pads 15 around its periphery. The polyimide printed circuit board 14. or interposer 14. is attached to the integrated circuit chip 11 using a layer of adhesive 12. such as a layer of epoxy adhesive 12. for example.

Fig. 1b shows an assembled chip-size package 10 wherein the polyimide printed circuit board 14 is electrically attached to the integrated circuit chip 11 using a plurality of wire bonds 18 coupled between the respective pluralities of bond pads 13. 15. Referring to Fig. 1c. after the wire bonds 18 are formed between the polyimide printed circuit board 14 and the integrated circuit chip 11. the wire bonds 18 are encapsulated using an encapsulant 17. such as flexible epoxy or silicone. for example.

Fig. 2 is a perspective view of a fully assembled chip-size integrated circuit package 10. The encapsulant 17 is shown in phantom. The chip-size integrated circuit package 10 has the area array of solder bumps 16 exposed for reflow soldering.

Fig. 3 illustrates the chip-size integrated circuit package 10 of Fig. 2 assembled to a printed circuit board 21. The printed circuit board 21 has an area array of solder bumps 22 that matches the area array of solder bumps 16 on the chip-size integrated circuit package 10. The chip-size integrated circuit package 10 and the printed circuit board 21 are electrically connected together by reflowing the solder bumps 16. 22 to form the electrical interconnections therebetween.

Thus. the present invention provides for a chip-size package 10 formed using a polyimide printed circuit board interposer 14. It is believed that the present invention

may be built for a relatively low cost than prior art chip-size packages because the present invention has fewer processing steps and has lower material costs. The present invention also uses more common and lower cost processing equipment than is used to produce prior art chip-size packages.

The present invention converts a single, unpackaged bare integrated circuit chip 11, for example, into a packaged chip 20 no larger in area than the bare chip 11. The present invention uses readily available printed circuit board materials and technology. The chip size package 10 uses the low cost printed circuit board interposer 14 with exposed, lower layers having wire bond pads 13, 15. The wire bond pads 13, 15 are sufficiently lower than the solder bumps 16 on top of the interposer 14, and therefore, wire bonds 18 to the wire bond pads 13, 15 are encapsulated without exceeding the height of the top printed circuit board 14 which must remain flat for soldering.

The present invention thus converts a bare chip 11 into a chip size package 10. The chip size package 10 may be assembled in a manner similar to surface mount devices which are soldered to printed circuit boards. The chip size package 10, however, takes up only 10-20% of the area of conventionally packaged chips 11 fabricated as surface mount devices.

The present invention packages the chip 11 within the internal surface area of the bare chip 11. Because the chip size package 10 takes up no additional area than the bare chip 11, it is believed to be the smallest two-dimensional integrated circuit package 10 that has yet been developed.

The chip size package 10 provides mechanical and environmental protection for the fragile integrated circuit chip 11. The chip size package 10 also converts a fine pitch peripheral pad integrated circuit 11 into a packaged, courser pitch area array device, permitting it to be easily tested, burned in, and assembled to standard printed circuit boards 21 using existing, common equipment used in the industry.

The present invention permits integrated circuits to be packaged in the smallest area possible, which is no larger than area of the integrated circuit 11. The chip size package 10 provides for a robust packaging structure that is suitable for a variety of commercial and military applications, including automotive electronics, for example.

Thus, a chip-size package formed using a polyimide printed circuit board interposer has been disclosed. It is to be understood that the described embodiment is merely illustrative of some of the many specific embodiments which represent applications of the principles of the present invention. Clearly, numerous and other arrangements can be readily devised by those skilled in the art without departing from the scope of the invention.

CLAIMS

What is claimed is:

1. A chip-size integrated circuit package comprising:

an integrated circuit chip having a plurality of peripheral bond pads:

a printed circuit board having a plurality of solder bumps formed on a top surface thereof and a plurality of bond pads around its periphery;

a layer of adhesive disposed between the polyimide printed circuit board and the integrated circuit chip to secure them together;

a plurality of wire bonds electrically connected between selected bond pads of the integrated circuit chip and the printed circuit board: and

an encapsulant for encapsulating the wire bonds and bond pads of the integrated circuit chip and the printed circuit board.

2. The package of Claim 1 wherein the integrated circuit chip comprises a silicon integrated circuit chip.

3. The package of Claim 1 wherein the printed circuit board comprises a polyimide printed circuit board.

4. The package of Claim 1 wherein the layer of adhesive comprises a layer of epoxy adhesive.

5. The package of Claim 1 wherein the encapsulant comprises flexible epoxy.

6. The package of Claim 1 wherein the encapsulant comprises silicone.

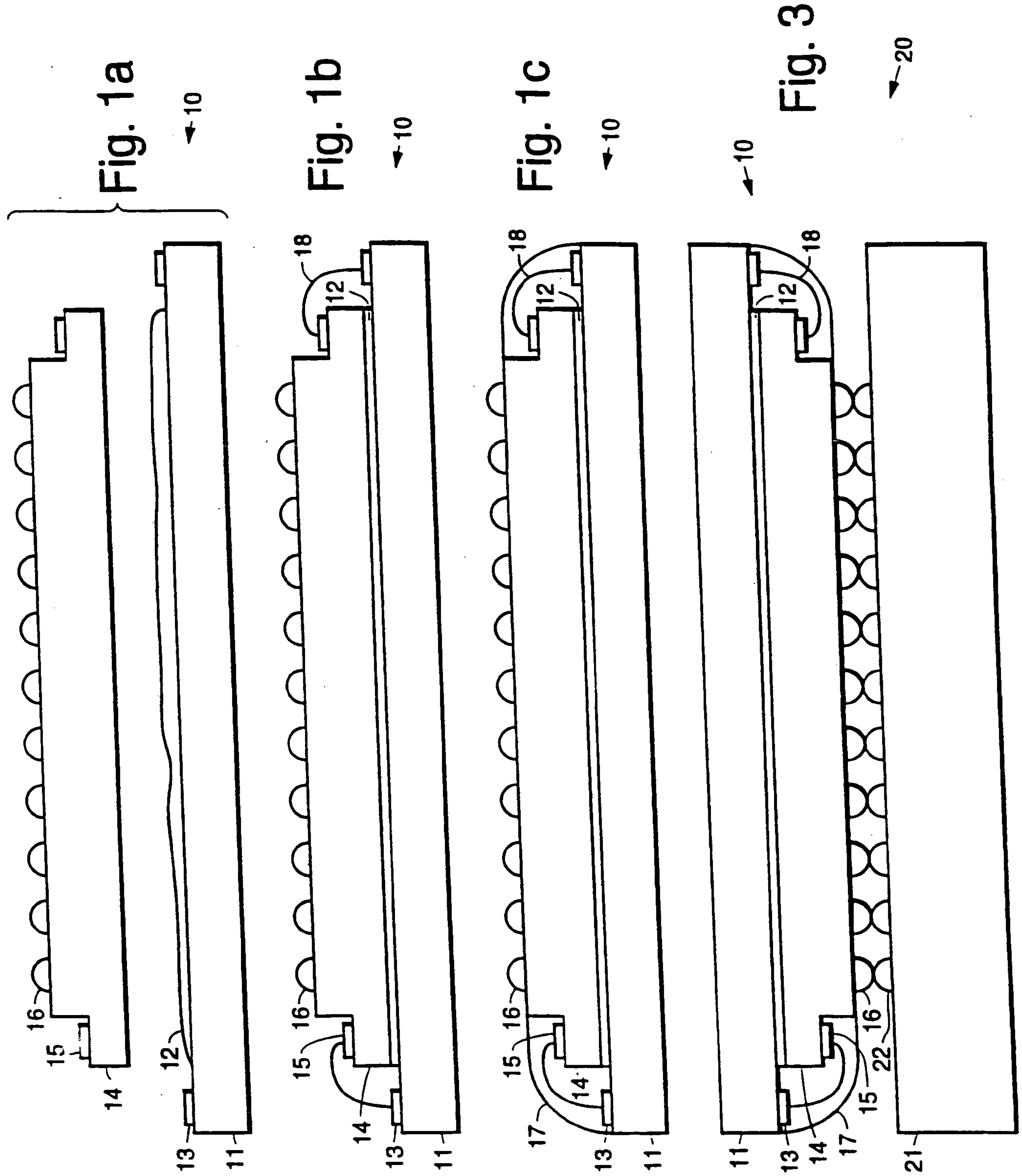
Fig. 1a
Fig. 1b
Fig. 1c
Fig. 3
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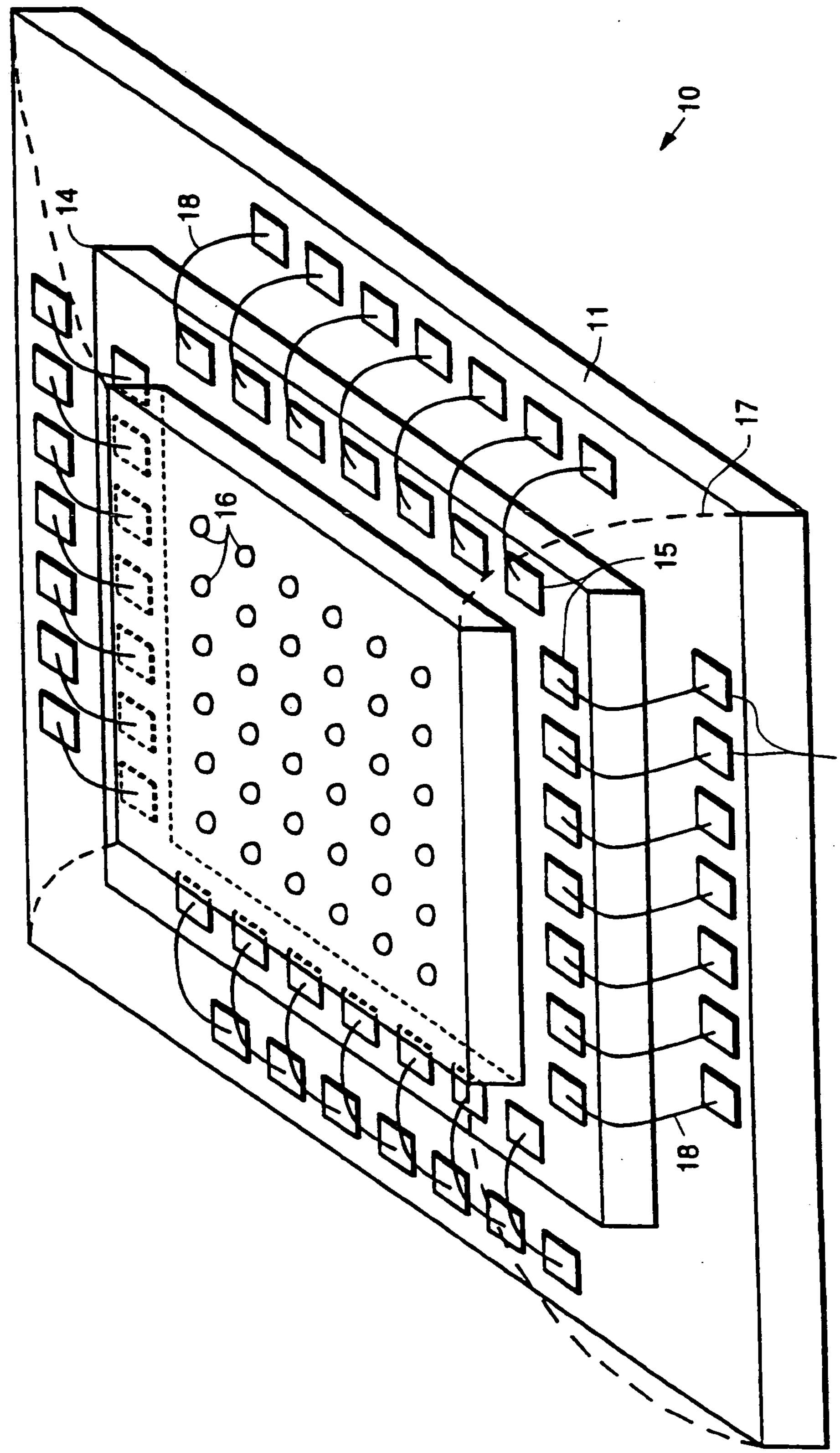

Fig. 2

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/US 98/20467

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/498

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 633 785 A (PARKER ROBERT H ET AL) 27 May 1997 see the whole document	1-6
A	US 5 777 391 A (NISHI KUNIHIKO ET AL) 7 July 1998 see the whole document & JP 08 227908 A (...)	1-6
P,X	US 5 714 800 A (THOMPSON PATRICK F) 3 February 1998 see the whole document	1-6

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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INTERNATIONAL SEARCH REPORT

..formation on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5633785 A	27-05-1997	NONE	
US 5777391 A	07-07-1998	JP 8227908 A	03-09-1996
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